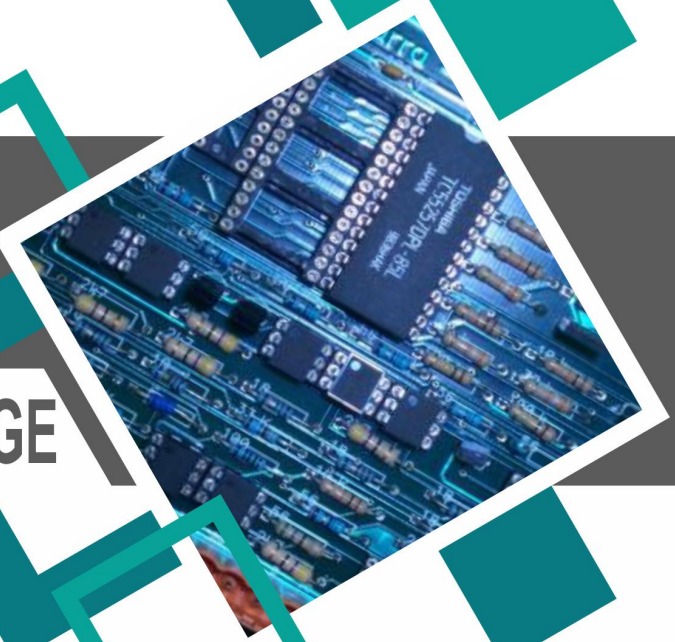
M.Sc. PHYSICS LAB MANUAL

1st Semester



Prepared By

Dept. of Pure & Applied Science

Physics

MIDNAPORE CITY COLLEGE

Course No: PHS 195: Electronics Practical-I

Credit: 4, Marks: 50

Experiment-1

AIM: To develop a filter circuit and to find out frequency response characteristics:

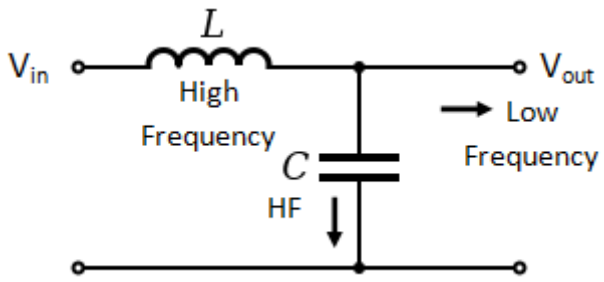
Theory and Circuit diagram:

An LC circuit, also called a resonant circuit, tank circuit, or tuned circuit, is an electric circuit consisting of an inductor, represented by the letter L, and a capacitor, represented by the letter C, connected together. The circuit can act as an electrical resonator, an electrical analogue of a tuning fork, storing energy oscillating at the circuit's resonant frequency.

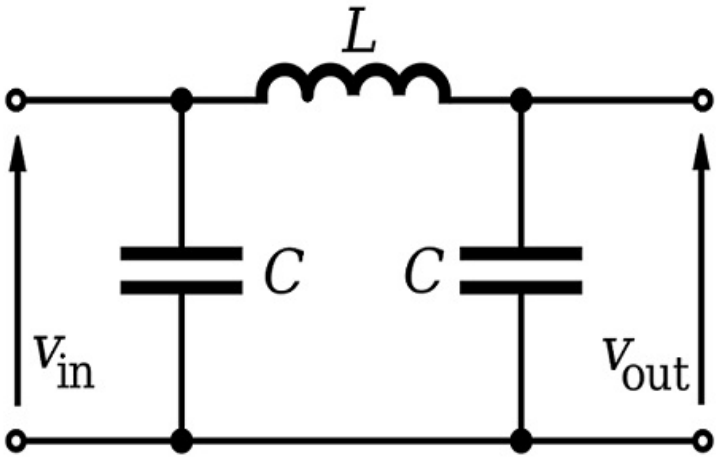
LC circuits are used either for generating signals at a particular frequency, or picking out a signal at a particular frequency from a more complex signal; this function is called a band pass filter. They are key components in many electronic devices, particularly radio equipment, used in circuits such oscillator, filter, tuners and frequency mixer.

Resonance occurs when an LC circuit is driven from an external source at an angular frequency ω_0 at which the inductive and capacitive reactance are equal in magnitude. The frequency at which this equality holds for the particular circuit is called the resonant frequency. The resonant frequency of the LC circuit is given by the following equation.

$$W_0 = 1/\sqrt{LC} \quad \text{.....(1)}$$



Circuit diagram of L type filter



Circuit diagram of π type filter

Experimental Data

1. **Frequency response of L type filter**

Table-1

V_i = 1 Volt (peak-peak), L=10mH, C=0.1μF

Frequency	Output Voltage(V_o)in Volt	Gain (V_o/V_i)	Gain in dB [20log(V_o/V_i)]

Table-2

V_i = 1 Volt (peak-peak), L=15mH, C=0.01μF

Frequency	Output Voltage(V_o)in Volt	Gain (V_o/V_i)	Gain in dB [20log(V_o/V_i)]

2. **Frequency response of π type filter**

Table-3

V_i = 1 Volt (peak-peak), L=10mH, C=0.1μF

Frequency	Output Voltage(V_o)in Volt	Gain (V_o/V_i)	Gain in dB [20log(V_o/V_i)]

Table-4

V_i = 1 Volt (peak-peak), L=15mH, C=0.01μF

Frequency	Output Voltage(V_o)in Volt	Gain (V_o/V_i)	Gain in dB [20log(V_o/V_i)]

Precautions and Discussions

1. Here the frequency responses of L type and π type filter are studied.
2. All the connections should be checked properly before starting the experiment.
3. Ensure that the system is properly ground.

Experiment-2

AIM: a) To Draw the drain and transfer characteristics of a given FET.

b) To find the drain resistance (r_d) amplification factor (μ) and Tran conductance (g_m) of a given FET.

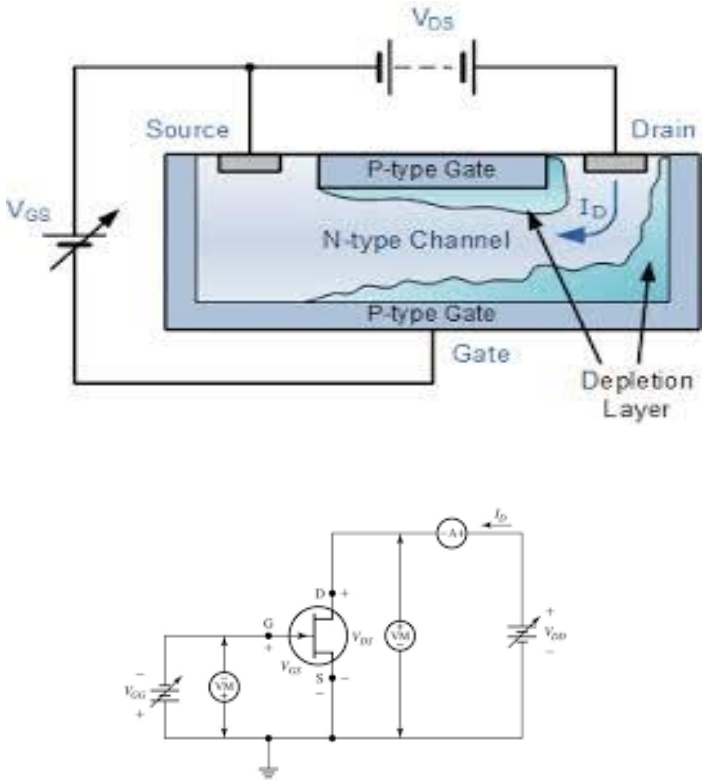
APPARATUS: FET (BFW-10), Regulated power supply, Voltmeter (0-20V), Ammeter (0-100mA), Bread Board, Connecting Wires.

Theory and circuit diagram: The Field Effect Transistor or Simply FET uses the voltage that is applied to their input terminal, called the Gate to control the current flowing through them resulting in the output current being proportional to the input voltage, the Gates to source junction of the FET is always reversed biased. As their operation relies on an electric field (hence the name field effect) generated by the input Gate voltage, this then makes the Field Effect Transistor a "VOLTAGE" operated device. The Field Effect Transistor is a three terminal unipolar semiconductor device that has very similar characteristics to those of their Bipolar Transistor counterpart's i.e., high efficiency, instant operation, robust and cheap and can be used in most electronic circuit applications to replace their equivalent bipolar junction transistors (BJT). The Field Effect Transistor has one major advantage over its standard bipolar transistor, in that input impedance, (R_{in}) is very high, (thousands of Ohms). This very high input impedance makes them very sensitive to input voltage signals. There are two basic configurations of junction field effect transistor, the N-channel JFET and the P-channel JFET. The N-channel JFET's channel is doped with donor impurities meaning that the flow of current through the channel is negative (hence the term N-channel) in the form of electrons. A FET is a three terminal device, having the characteristics of high input impedance and less noise, the Gate to Source junction of the FET is always reverse biased.

In amplifier application, the FET is always used in the region beyond the pinch-off.

The characteristics curves example shown above, shows the four different regions of operation for a JFET and these are given as: Ohmic Region-When VGS =0 the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor. Cut-off region- This is also known as the pinch-off region were the Gate Voltage, VGS is

sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum. Saturation or Active Region – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (VGS) while the Drain-Source voltage, (VDS) has little or no effect. Breakdown Region-The voltage between the Drain and the Source, (VDS) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current.



Circuit diagram to study FET characteristics

PROCEDURE:

1. All the connections are made as per the circuit diagram.

2. To plot the drain characteristics keep V_{GS} constant at 0V.

3. Vary the V_{DS} and observe the values of V_{DS} and ID. 4. Repeat the above steps 2, 3 for different values of V_{GS}.

5. All the readings are tabulated.

6. To plot the transfer characteristics, keep V_{DS} constant at 1V.

7. Vary V_{GS} and observe the values of V_{GS} and ID.

8. Repeat steps 6 and 7 for different values of V_{DS}.

9. The readings are tabulated.

10. From drain characteristics, calculate the values of dynamic resistance (r_d) by using the formula $r_d = \Delta V_{DS} \Delta I_D$

11. From transfer characteristics, calculate the value of trans conductance (g_m) By using the $g_m) = \Delta I_D / \Delta V_{GS}$.

12. Amplification factor (μ) = $\Delta V_{DS} / \Delta V_{GS}$.

Experimental Data

Table-1

DRAIN CHARACTERISTICS

V_{GS}=0V		V_{GS}=-0.5 V		V_{GS}=-1 V		V_{GS}=-1.5 V		V_{GS}=-2.0 V	
V_{DS} in volts	I_D in mA	V_{DS} in volts	I_D in mA	V_{DS} in volts	I_D in mA	V_{DS} in volts	I_D in mA	V_{DS} in volts	I_D in mA

Table-2

TRANSFER CHARACTERISTICS

V_{DS} = 0.5 V		V_{DS}= 1.0 V		V_{DS} =1.5 V		V_{DS} =2.0 V	
V_{GS} in volts	I_D in mA	V_{GS} in volts	I_D in mA	V_{GS} in volts	I_D in mA	V_{GS} in volts	I_D in mA

Precautions and Discussions

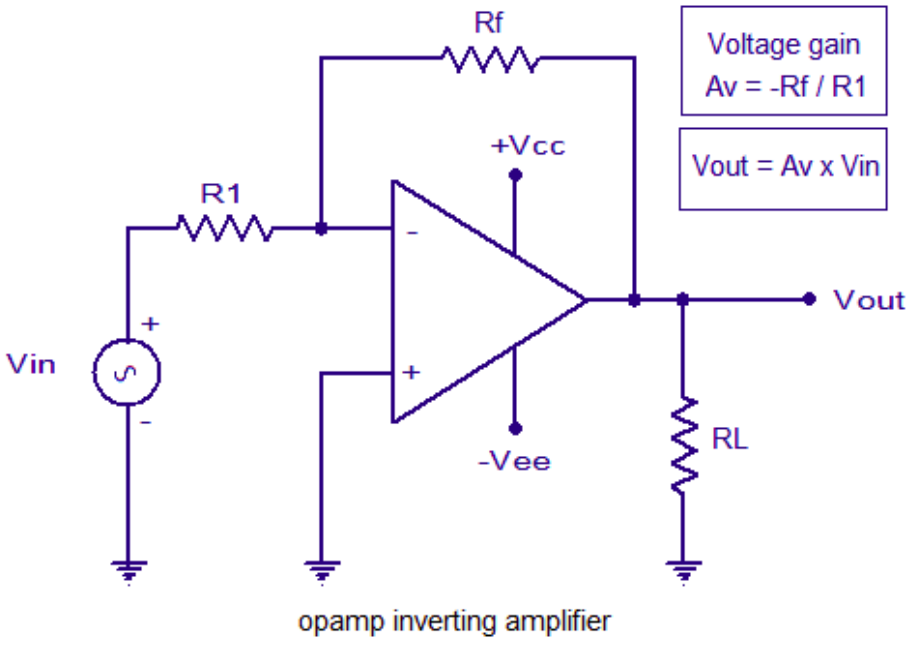
1. Here drain characteristics and transfer characteristics of BFW -10 JFET are measured.
2. Identify terminals of the JEFT properly.
3. Before starting experiment all the connections should be checked properly.
4. Maximum allowable values of V_{DS} and I_D should never be exceeded.

Experiment-3

AIM: To obtain the frequency response characteristics of an inverting Op-Amp and find out its band width.

Apparatus Required: Bread Board, 741 IC, ±12V supply, Resistors and connecting leads.

Theory and Circuit diagram: An inverting amplifier using Op-Amp is a type of amplifier using Op-Amp where the output waveform will be phase opposite to the input waveform. The input waveform will be amplifier by the factor Av (voltage gain of the amplifier) in magnitude and its phase will be inverted. In the inverting amplifier circuit the signal to be amplified is applied to the inverting input of the Op-Amp through the input resistance R_1. R_f is the feedback resistor. R_f and R_{in} together determine the gain of the amplifier. Inverting operational amplifier gain can be expressed using the equation $A_v = -R_f/R_1$. Negative sign implies that the output signal is negated. The circuit diagram of a basic inverting amplifier using Op-Amp is shown below.



opamp inverting amplifier

Procedure:

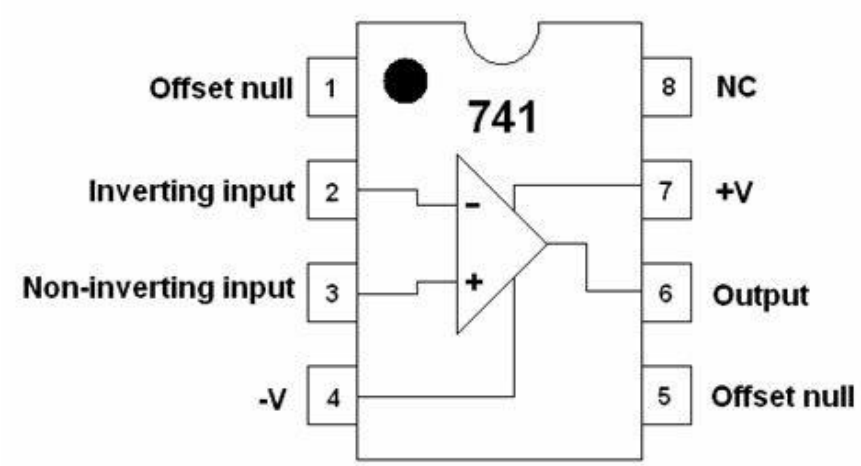
1) Connect the circuit for inverting, amplifier on a breadboard.

2) Connect the input terminal of the op-amp to function generator and output terminal to CRO.

3) Feed input from function generator and observe the output on CRO.

4) For frequency response characteristics choose an input voltage such that the output voltage is the order of 0.5 volt then vary the frequency and note down the output voltage.

5) Draw the input and output waveforms on graph paper.



Pin diagram of Op-Amp IC

Experimental Data for Linearity characteristics

Table-1

Frequency of input signal =1 kHz; Gain=1

Input Voltage in Volt	Output Voltage in Volt

Table-2

Frequency of input signal =1 kHz; Gain=10

Input Voltage in Volt	Output Voltage in Volt

Experimental Data for Frequency response characteristics

Table-3

Input voltage (V_i) fixed at ....volt; Gain = 1

Frequency (f) of input signal	Output voltage (V_O)	Gain (V_O/ V_i)	Gain in dB

Table-4

Input voltage (V_i) fixed at ....volt; Gain=10

Frequency (f) of input signal	Output voltage (V_O)	Gain (V_O/ V_i)	Gain in dB

Precautions and Discussions

1. Here the frequency response characteristic of an Op-Amp (IC 741) in inverting mode is studied and the band width is determined.
2. Before switching on the power supply, it should be ensured that all the pin connections are made properly.
3. Before taking reading ensure that the IC is connected in inverting mode.
4. After completing the experiment power off all the sources.

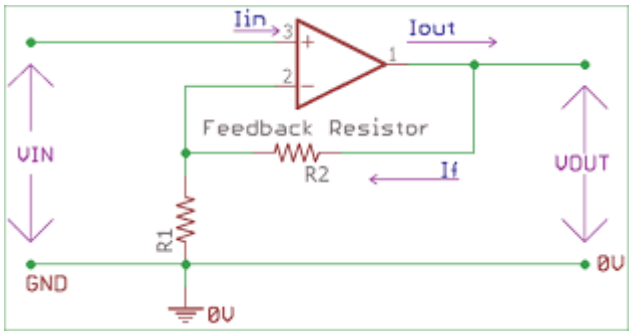
Experiment-4

AIM: To obtain the frequency response characteristics of a non-inverting Op-Amp and find out its band width.

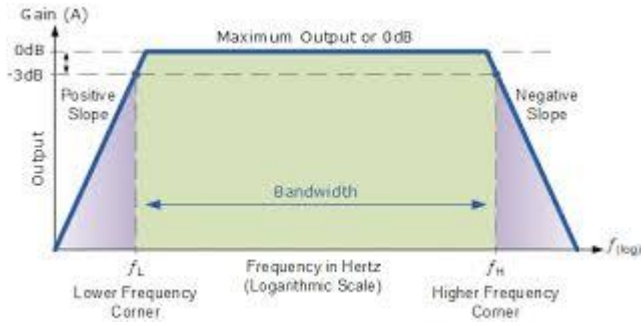
Apparatus Required: Bread Board, 741 IC, ±12V supply, Resistors and connecting leads.

Theory and Circuit diagram:

Formula- Output voltage $V_0 = (1+R_2/R_1)V_{IN}$



Circuit diagram of non-inverting-Op-Amp



Bandwidth diagram

Procedure:

1) Connect the circuit for non-inverting, amplifier on a breadboard.

2) Connect the input terminal of the op-amp to function generator and output terminal to CRO.

3) Feed input from function generator and observe the output on CRO.

4) For frequency response characteristics choose an input voltage such that the output voltage is the order of 0.5 volt then vary the frequency and note down the output voltage.

5) Draw the input and output waveforms on graph paper.

Experimental Data for Linearity characteristics

Table-1

Frequency of input signal =1 kHz; Gain=2

Input Voltage in Volt	Output Voltage in Volt

Table-2

Frequency of input signal =1 kHz; Gain=11

Input Voltage in Volt	Output Voltage in Volt

Experimental Data for Frequency response characteristics

Table-3

Input voltage (V_i) fixed at ....volt; Gain=2

Frequency (f) of input signal	Output voltage (V_O)	Gain (V_O/ V_i)	Gain in dB

Table-4

Input voltage (V_i) fixed at ....volt; Gain=11

Frequency (f) of input signal	Output voltage (V_O)	Gain (V_O/ V_i)	Gain in dB

Table-5

Input voltage (V_i) fixed at ....volt; Gain=34

Frequency (f) of input signal	Output voltage (V_O)	Gain (V_O/ V_i)	Gain in dB

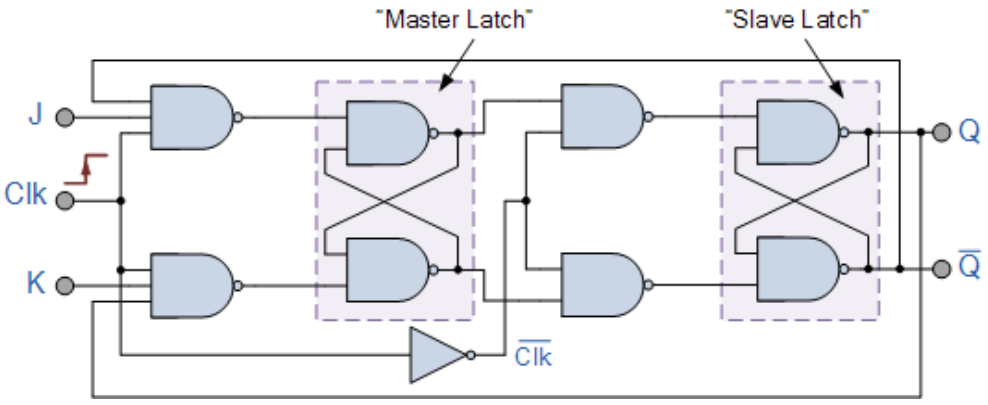
Precautions and Discussions

1. Here the frequency response characteristic of an Op-Amp (IC 741) in non-inverting mode is studied and the band width is determined.
2. Before switching on the power supply it should be ensured that all the pin connections are made properly.
3. Before taking reading ensure that the IC is connected in non-inverting mode.

Experiment-5

Theory and Circuit diagram:

The master-slave flip-flop eliminates all the timing problems by using two SR flip-flops connected together in a series configuration. One flip-flop acts as the "Master" circuit, which triggers on the leading edge of the clock pulse while the other acts as the "Slave" circuit, which triggers on the falling edge of the clock pulse. This results in the two sections, the master section and the slave section being enabled during opposite half-cycles of the clock signal.

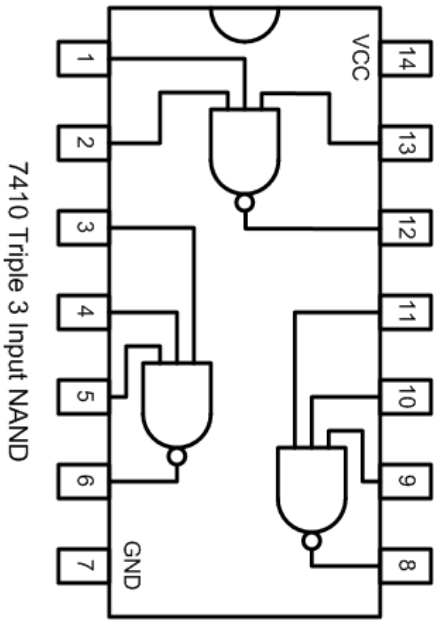


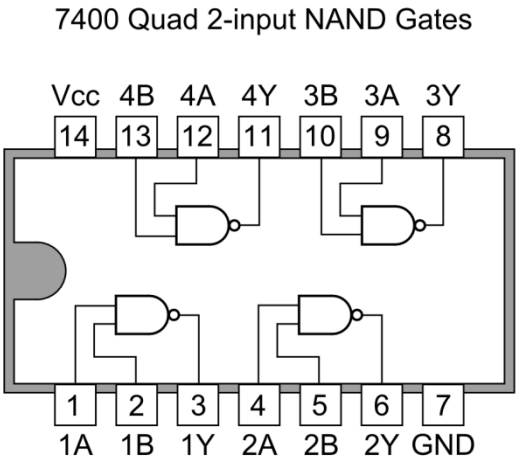
The Master-Slave JK Flip Flop

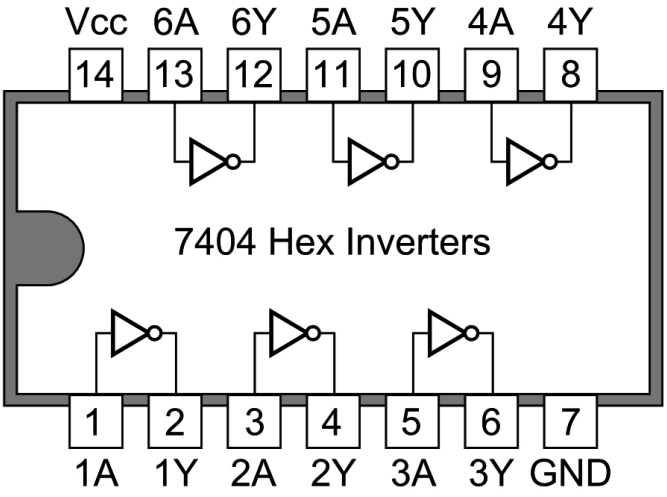
Truth Table

J_n	K_n	Q_n	$\bar{Q}_n$	Q_{n+1}
0	0	0	1	Q_n
0	0	1	0	Q_n
1	0	0	1	1
1	0	1	0	Q_n
0	1	0	1	Q_n
0	1	1	0	0
1	1	0	1	1
1	1	1	0	0

Pin Diagram of IC 7400, 7404, 7410







Precautions and Discussions

1. The pins should be connected properly.
2. The IC should be checked before connection.
3. Connect the IC pins properly with V_{cc} and ground terminal.
4. If there is any initial error in meters check them properly.
5. After completing the experiment power off all the sources.