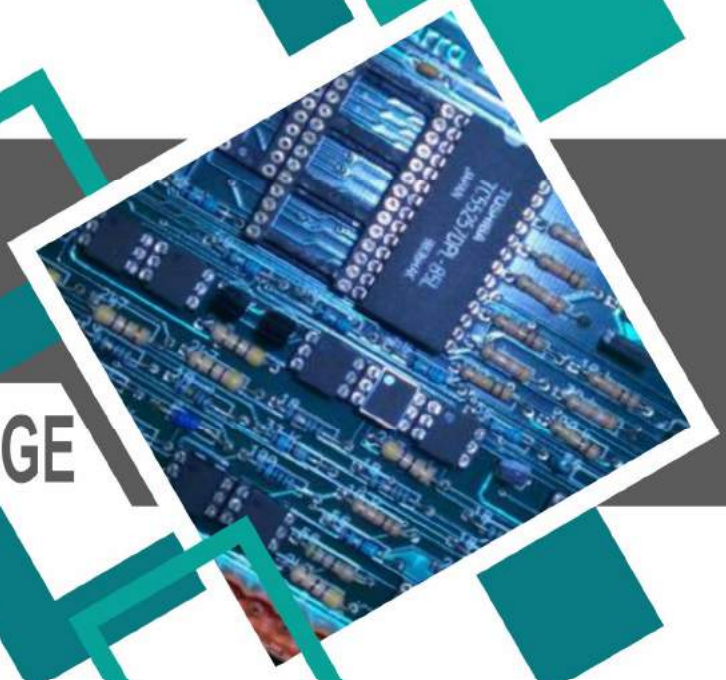
B.Sc. PHYSICS LAB MANUAL

3rd Semester



Prepared By

Pure & Applied Sciences

Physics

MIDNAPORE CITY COLLEGE

Course No: C7P: Digital Systems and Applications Lab

Credit: 2

Experiment-1

AIM: To measure (a) Voltage, and (b) Time period of a periodic waveform using CRO:

Theory:

Cathode ray oscilloscope is one of the most useful electronic equipment, which gives a visual representation of electrical quantities, such as voltage and current waveforms in an electrical circuit. It utilizes the properties of cathode rays of being deflected by an electric and magnetic fields and of producing scintillations on a fluorescent screen. Since the inertia of cathode rays is very small, they are able to follow the alterations of very high frequency fields and thus electron beam serves as a practically inertia less pointer. When a varying potential difference is established across two plates between which the beam is passing, it is deflected and moves in accordance with the variation of potential difference. When this electron beam impinges upon a fluorescent screen, a bright luminous spot is produced there which shows and follows faithfully the variation of potential difference. When an AC voltage is applied to Y-plates, the spot of light moves on the screen vertically up and down in straight line. This line does not reveal the nature of applied voltage waveform. Thus to obtain the actual waveform, a time-base circuit is necessary. A time-base circuit is a circuit which generates a saw-tooth waveform. It causes the spot to move in the horizontal and vertical direction linearly with time. When the vertical motion of the spot produced by the Y-plates due to alternating voltage, is superimposed over the horizontal sweep produced by X-plates, the actual waveform is traced on the screen.

Apparatus:- A C.R.O and a signal generator.

Procedure:-

Study of waveforms: To study the waveforms of an A.C voltage, it is led to the y – plates and the time base voltage is given to the X-plates. The size of the figure displayed on the screen, can be adjusted suitably by adjusting the gain controls. The time base frequency can be changed, so as to accommodate one, two or more cycles of the signal. There is a provision in C.R.O to obtain a sine wave or a square wave or a triangular wave. Measurement of D.C.Voltage : - Deflection on a CRO screen is directly proportional to the voltage applied to the deflecting plates. Therefore, if the screen is first calibrated in terms of known voltage. i.e. the deflection sensitivity is determined , the direct voltage can be measured by applying it between a pair of deflecting plates. The amount of deflection so produced multiplied by the deflection sensitivity, gives the value of direct voltage.

Measurement of A.C voltage: - To measure the alternating voltage of sinusoidal waveform, The A.C. signal, from the signal generator, is applied across the y – plates. The voltage(deflection) sensitivity band switch (Y-plates) and time base band switch (X-plates) are adjusted such that a steady picture of the waveform is obtained on the screen. The vertical height (l) i.e. peak-to-peak height is measured. When this peak-to-peak height (l) is multiplied by the voltage(deflection) sensitivity (n) i.e. volt/div, we get the peak-to-peak voltage (2Vo). From this we get the peak voltage (Vo). The rms voltage Vrms is equal to Vo/ 2 . This rms voltage Vrms is verified with rms voltage value, measured by the multi-meter.

Measurement of frequency: - An unknown frequency source (signal generator) is connected to y- plates of C.R.O. Time base signal is connected to x – plates(internally connected) . We get a sinusoidal wave on the screen, after the adjustment of voltage sensitivity band switch (Y-plates) and time base band switch (X-plates). The horizontal length(l) between two successive peaks is noted. When this horizontal length (l) is multiplied by the time base(m) i.e. sec/div , we get the time-period(T).The reciprocal of the time-period(1/T) gives the frequency(f). This can be verified with the frequency, measured by the multi-meter.

Results : -

Table-1

Voltage measurement:

S.No	Peak to peak (Vertical) length. (Divisions) (l)	Voltage Sensitivity. (Volt/Div) (n)	Peak to peak Voltage $2V_o$=nxl (volts)	Peak voltage V_o=($2V_o$/2) (volts)	Rms Voltage V_{rms}=($V_o/\sqrt{2}$) (volts)	Measured voltage with Multi-meter (volts)
1.						
2.						
3.						
4.						
5.						

Table-2

Frequency measurement:

S.No.	Peak to peak (Horizontal) length (Divisions) (l)	Time-base Sec/Div (m)	Time-period T = mxl Sec.	Measured frequency f = 1/T Hz	Applied Frequency Hz
1.					
2.					
3.					
4.					
5.					
6.					

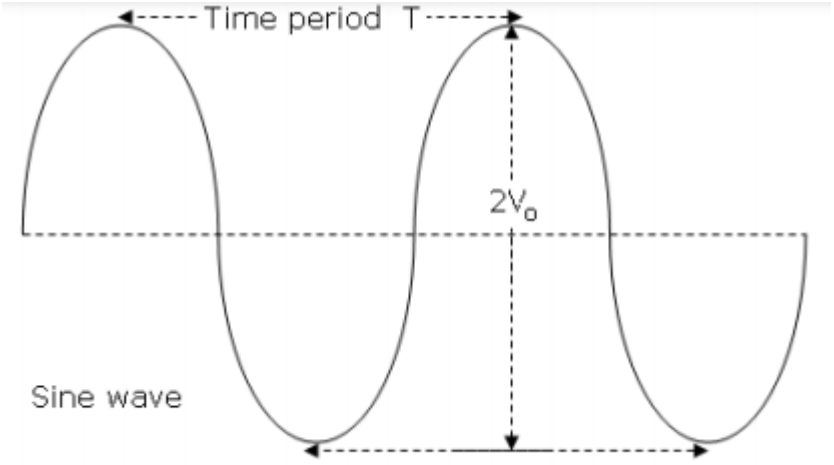
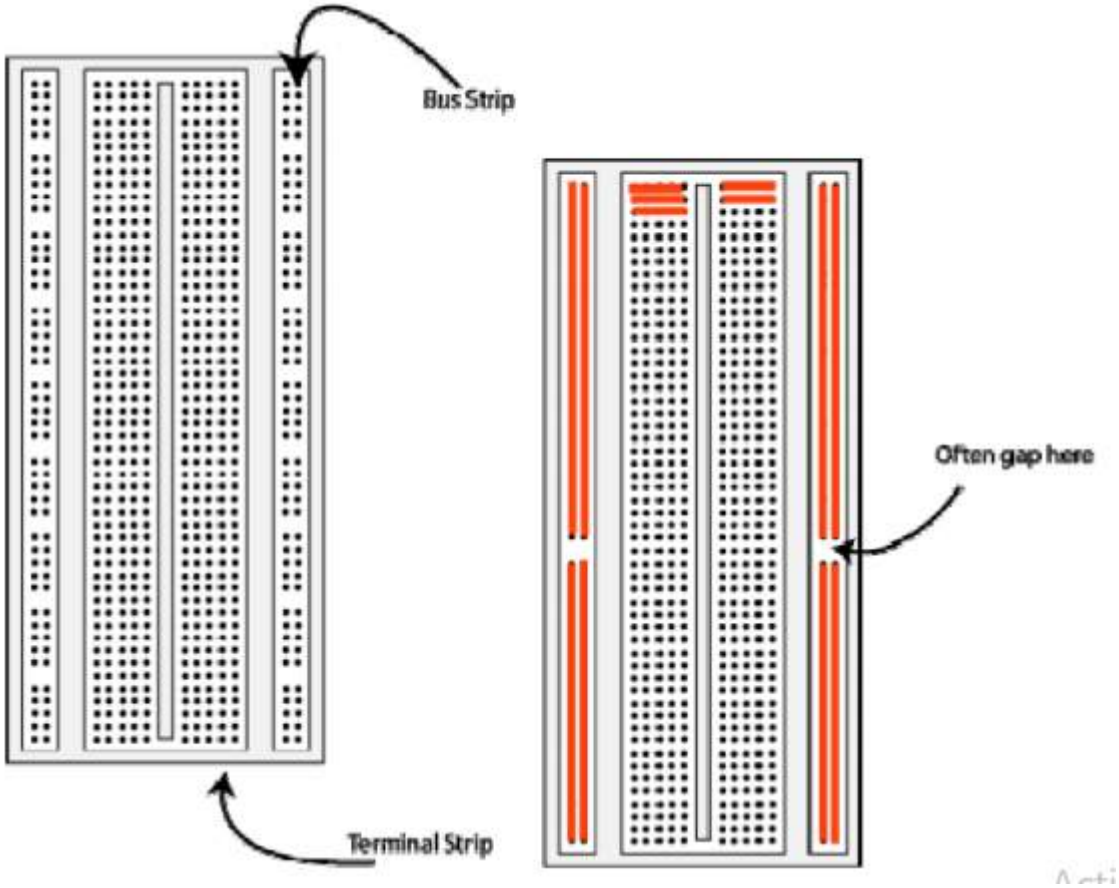


Fig `1: A Sine Wave

Precautions: - 1) The continuity of the connecting wires should be tested first. 2) The frequency of the signal generator should be varied such that steady wave form is formed.

BREADBOARD

The breadboard consists of two terminal strips and two bus strips (often broken in the centre). Each bus strip has two rows of contacts. Each of the two rows of contacts is a node. That is, each contact along a row on a bus strip is connected together (inside the breadboard). Bus strips are used primarily for power supply connections, but are also used for any node requiring a large number of connections. Each terminal strip has 60 rows and 5 columns of contacts on each side of the centre gap. Each row of 5 contacts is a node. You will build your circuits on the terminal strips by inserting the leads of circuit components into the contact receptacles and making connections with 22-26 gauge wire. There are wire cutter/strippers and a spool of wire in the lab. It is a good practice to wire +5V and 0V power supply connections to separate bus strips.



Experiment 2

AIM: (a) To design a Logic Gate using a Discreet Components (Diode and Transistors).
(b) Realization Of Gates Using Integrated Circuits.

Apparatus:

1. Breadboard
2. Resistors 10k, 1k, 220ohms
3. Transistors 2N2222 (NPN)
4. Diodes 1N 4001
5. AND Gate IC 7408
6. OR Gate IC 7432
7. NOT Gate IC 7404
8. NAND Gate IC 7400
9. NOR Gate IC 7402
10. Connecting wires
11. DMM
12. LED

Theory:

OR Gate:

The operation of these gates is to consider the diode as a simple switch, which is closed (on) when the voltage on one side (the anode) is higher than the other (the cathode). The current then flows in the direction of the arrow in the diode's circuit diagram symbol. The figure 1(a) shows the logic symbol, my discrete component implementation, and the truth table. In an OR gate, the output is "1" (high) if either of the inputs are "1". In this diagram, if either of the inputs has a "high" voltage, its diode will conduct and current will flow to the output. A "high" voltage will develop across the resistor, equivalent to the input voltage minus 0.7V drop, as is usual across silicon diode junctions. If both of the inputs are low voltage "0", then the diodes don't conduct. In this instance the gate's output is tied low by the 10K resistor.

AND Gate:

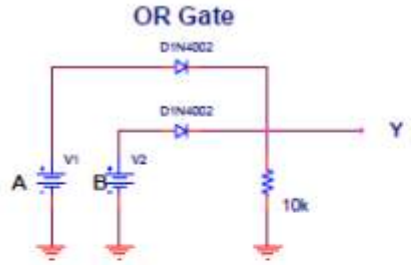
It's similar to the OR gate except that the diodes point in the other direction, and the resistor goes to +5V not ground. The output of an AND gate is "1" only if BOTH the inputs are "1". In

diode–resistor implementation, if either input is "low" voltage (logic "0") then the diode will conduct and the output is effectively shorted to ground. If both of the input voltages are "high" (logic "1") then neither of the diodes will conduct, so the output is not shorted to ground: it remains at +5V (logic "1") via the 10K resistor. This gives the desired result. Note that again, due to the silicon junction voltage, the actual "low" output voltage is 0.7V higher than the "low" input voltage.

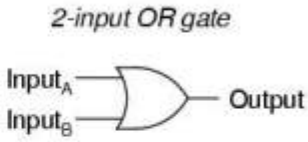
NOT Gate:

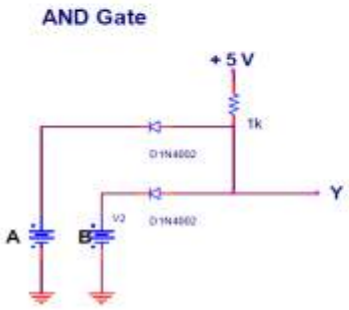
You cannot implement an inverting function with diodes and resistors alone. You also now need a transistor, to provide the inverting action. There's nothing particularly special about the transistor to be used, almost any small signal NPN transistor will suit, since it's driven into saturation (unbiased). If the voltage presented to the base of the transistor is above 0.7, the transistor will conduct which drags the output to logic "0", low voltage. If the input voltage is logic "0", then the transistor does not conduct, and the resistor will just tie the output to +5V. You always need that 10K current limiting resistor in the base, or excessive base-emitter current will destroy the transistor.

Circuit Diagrams:

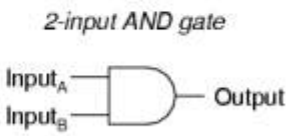


A	B	Y
0v	0v	0v
0v	5v	5v
5v	0v	5v
5v	5v	5v

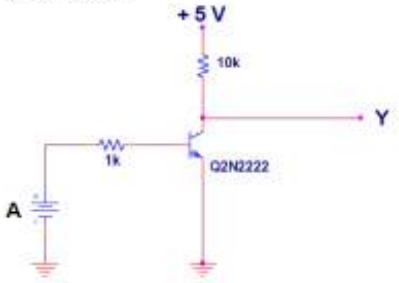




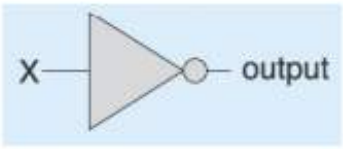
A	B	Y
0v	0v	0v
0v	5v	0v
5v	0v	0v
5v	5v	5v



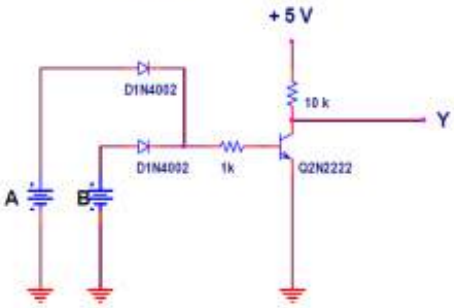
NOT Gate



A	Y
0v	5v
5v	0v

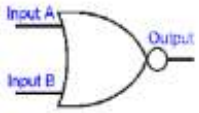


NOR Gate

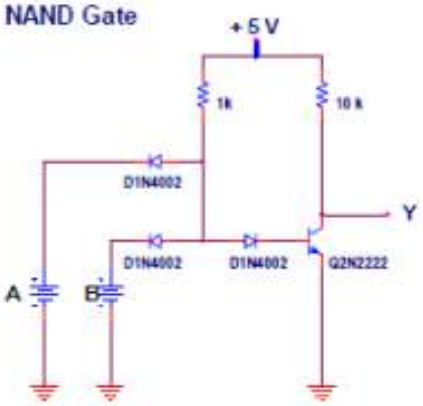


A	B	Y
0v	0v	5v
0v	5v	0v
5v	0v	0v
5v	5v	0v

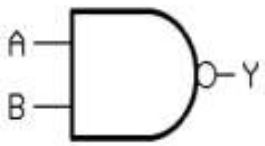
2-input NOR gate



NAND Gate



A	B	Y
0v	0v	5v
0v	5v	5v
5v	0v	5v
5v	5v	0v



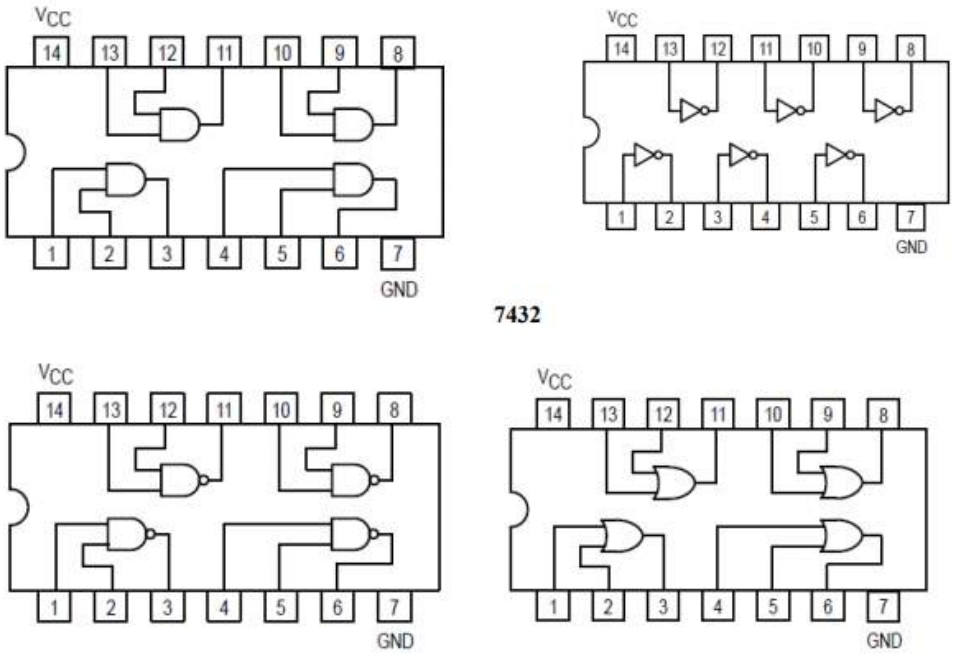


Fig: 2: Pin Configuration (a) AND Gate IC7408 (b) NOT Gate IC7404 (c) NAND Gate IC7400 (d) OR Gate IC.

Procedure:[a] REALIZATION OF GATES USING DISCRETE COMPONENTS

1. Connections are made as per the circuit diagram.
2. Switch on the power supply.
3. Apply different combinations of inputs and observe the outputs; compare the outputs with the truth tables.

[B] REALIZATION OF GATES USING INTEGRATED CIRCUITS

1. Place the IC on breadboard.
2. Connect Vcc and Gnd to the respective pins of IC Trainer Kit.
3. Connect the inputs to the input switches/logical switches.
4. Connect the output to the switches of O/p or LEDs.
5. Apply various combinations f inputs according to the truth table and observe condition of LEDs.
6. Disconnect output from LEDs and note down the corresponding multimeter voltage readings for various combinations of inputs.

Precautions: All the connections should be made properly. Result: Different logic gates are constructed and their truth tables are verified.

Conclusion:

Experiment 3

AIM: To verify and design AND, OR, NOT and XOR gates using NAND gates.

Apparatus: 1. Breadboard 2. NAND Gate IC 7400 3. NOR Gate IC 7402 4. Connecting wires 5. DMM 6. LEDs 7. Power Supply

Theory:

A binary variable can take the value of 0 or 1. A Boolean function is an expression formed with binary variables, the two binary operators OR and AND, and unary operator NOT, parentheses, and an equal sign. For a given value of the variables, the function can be either 0 or 1. Boolean function represented as an algebraic expression may be transformed from an algebraic expression into a logic diagram composed of AND, OR, and NOT gates. . Every Boolean function can be realized by a And-Or-Not gates i.e. using AOI logic.

NAND GATE is a universal gate. It is so called as because by using of this gate we can make any gate like not, or, and etc. by help of this gate we can also make multiplexers and de mux.

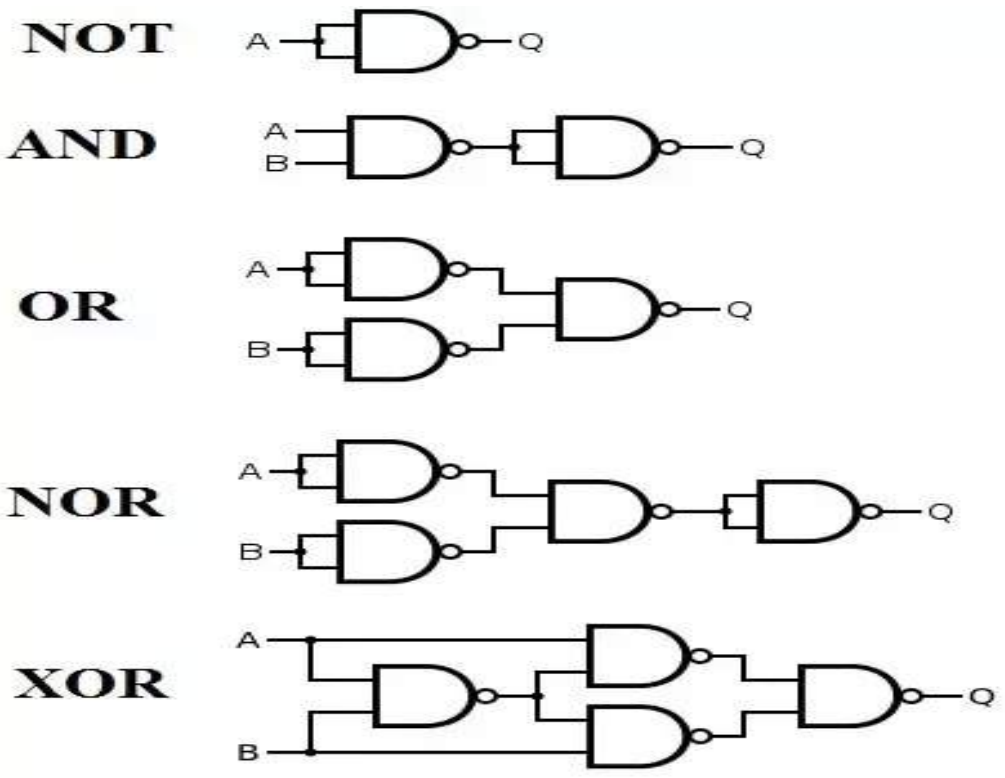


Fig: 1: Implementation of Basic Gates Using NAND Gate

Procedure:

1.Place the IC on breadboard.

2. Connect Vcc and Gnd to the respective pins of IC Trainer Kit.

3. Connect the inputs to the input switches/logical switches.

4. Connect the output to the switches of O/p or LEDs.

5. Apply various combinations f inputs according to the truth table and observe condition of LEDs.

6. Disconnect output from LEDs and note down the corresponding multimeter voltage readings for various combinations of inputs.

Precautions:

1. All the connections should be made properly.

2. Before the circuit connection it should be check out working condition of all the components and ICs.

Result:

Different logic gates are constructed and their truth tables are verified

Conclusion:

Experiment 4

AIM: To design a combinational logic system for a Half Adder and Full adder.

Apparatus:

1. Breadboard
2. Resistors 10k, 1k, 220ohms
3. IC's - 7486, 7432, 7408, 7400
4. Connecting wires

Theory:

Half adder:

The half adder is a combinational circuit which add two inputs: A and B, and generates a carry (C) and a sum (S).The half adder circuit truth table and circuit diagram is shown in figure 1.

Inputs		Outputs	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Truth table

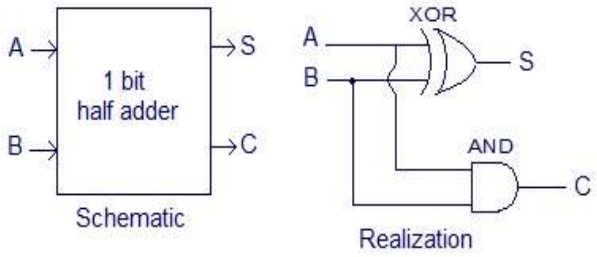


Fig1: Half adder with truth table

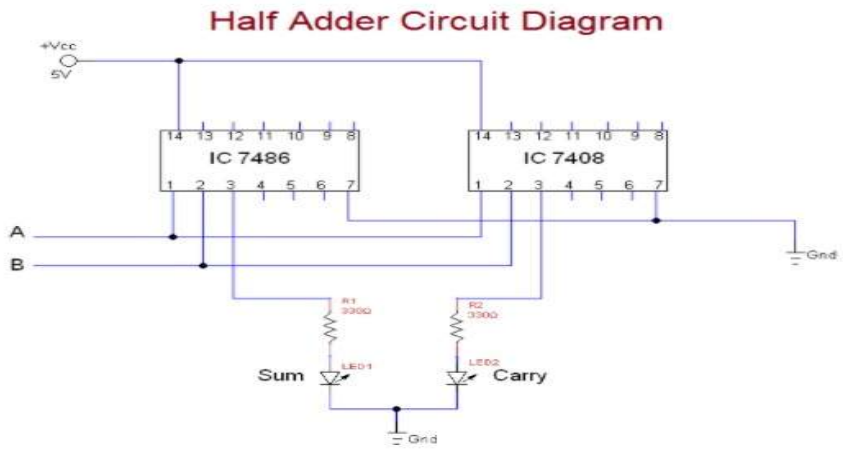


Fig2: Half adder circuit Diagram

Full adder:

Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM.

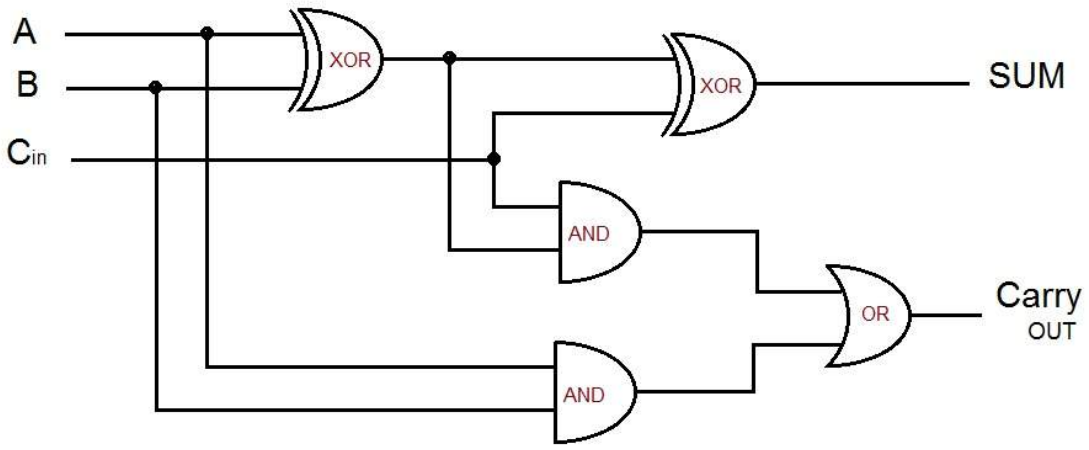


Fig3: Full adder

Table 2: Full Adder

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Procedure:

1. Verify the gates.
2. Make the connections as per the circuit diagram.
3. Switch on VCC and apply various combinations of input according to truth table.
4. Note down the output readings for half/full adder and half/full subtractor, Sum/difference and the carry/borrow bit for different combinations of inputs verify their truth tables.

Precautions:

1. All the connections should be made properly.

2. Before the circuit connection it should be check out working condition of all the components and ICs.

Result:

Conclusion:

Experiment 5

Aim: To design a J-K master-slave flip-flop and to verify its truth table

Theory and Circuit diagram:

The master-slave flip-flop eliminates all the timing problems by using two SR flip-flops connected together in a series configuration. One flip-flop acts as the "Master" circuit, which triggers on the leading edge of the clock pulse while the other acts as the "Slave" circuit, which triggers on the falling edge of the clock pulse. This results in the two sections, the master section and the slave section being enabled during opposite half-cycles of the clock signal.

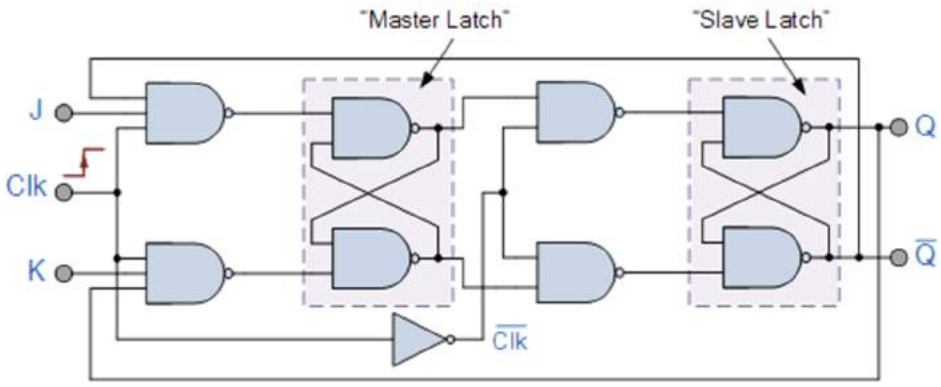
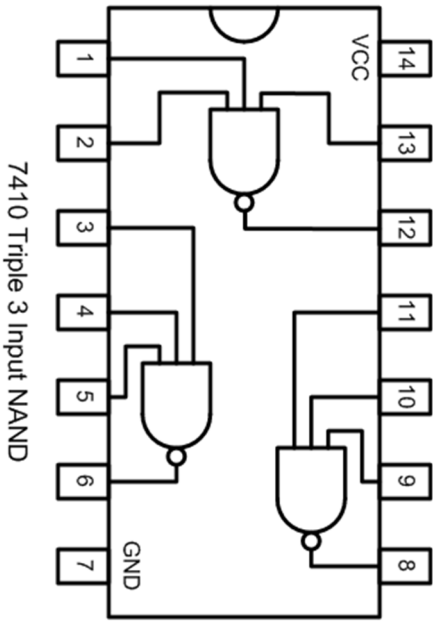


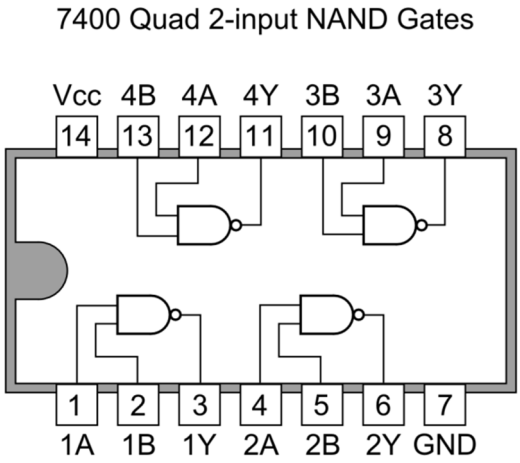
Fig 1: The Master-Slave JK Flip Flop

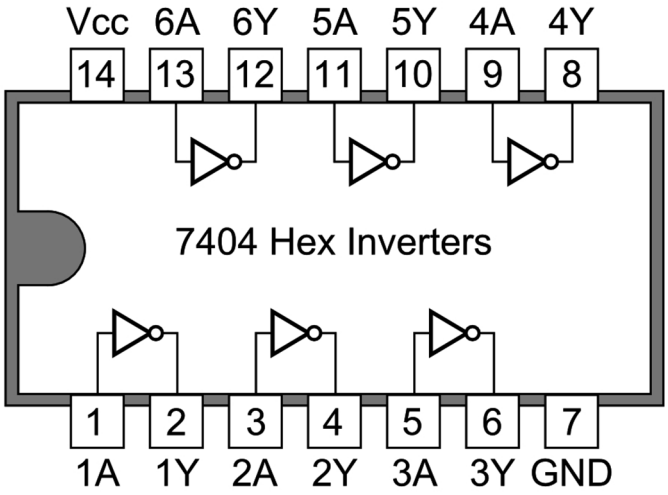
Truth Table

J_n	K_n	Q_n	$\bar{Q}_n$	Q_{n+1}
0	0	0	1	Q_n
0	0	1	0	Q_n
1	0	0	1	1
1	0	1	0	Q_n
0	1	0	1	Q_n
0	1	1	0	0
1	1	0	1	1
1	1	1	0	0

Pin Diagram of IC 7400, 7404, 7410







Precautions and Discussions:

1. The pins should be connected properly.
2. The IC should be checked before connection.
3. Connect the IC pins properly with $V_{cc}$and ground terminal.
4. If there is any initial error in meters check them properly.
5. After completing the experiment power off all the sources.

Experiment 6

AIM: To design an astablemultivibrator of given specifications using 555 Timer.

Theory:

IC 555 timer is an analog IC used for generating accurate time delay or oscillations. The entire circuit is usually housed in an 8-pin package as specified in figures 1 & 2 below. A series connection of three resistors inside the IC sets the reference voltage levels to the two comparators at 2/3 CC V and 1/3 CC V, the output of these comparators setting or resetting the flipflop unit. The output of the flip-flop circuit is then brought out through an output buffer stage. In the stable state the Q output of the flip-flop is high (ie Q low). This makes the output (pin 3) low because of the buffer which basically is an inverter.The flip-flop circuit also operates a transistor inside the IC, the transistor collector usually being driven low to discharge a timing capacitor connected at pin 7. The description of each pin s described below:

Pin 1: (Ground): Supply ground is connected to this pin.

Pin 2: (Trigger): This pin is used to give the trigger input in monostablemultivibrator. When trigger of amplitude greater than (1/3)Vcc is applied to this terminal circuit switches to quasi-stable state.

Pin 3: (Output)

Pin 4 (Reset): This pin is used to reset the output irrespective of input. A logic low at this pin will reset output. For normal operation pin 4 is connected to Vcc.

Pin 5 (Control): Voltage applied to this terminal will control the instant at which the comparator switches, hence the pulse width of the output. When this pin is not used it is bypassed to ground using a 0.01µF capacitor.

Pin 6 (Threshold): If the voltage applied to threshold terminal is greater than (2/3)VCC, upper comparator switches to +Vsat and flip-flop gets reset.

Pin 7: (Discharge): When the outputis low, the external capacitor is discharged through this pin

Pin 8 (VCC): The power supply pin

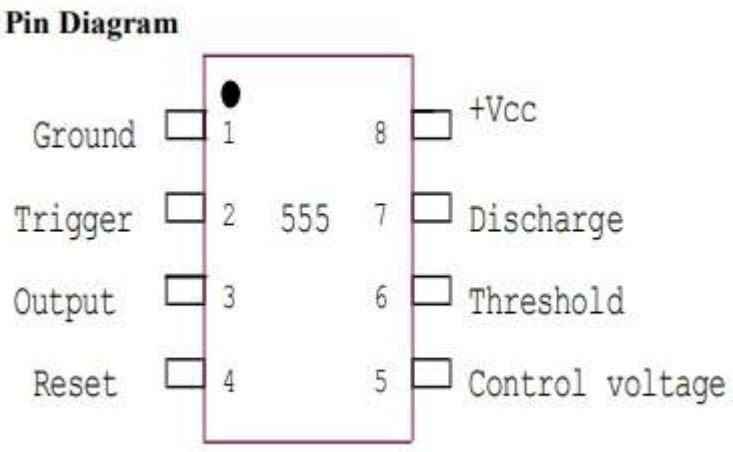


Fig1 IC 555

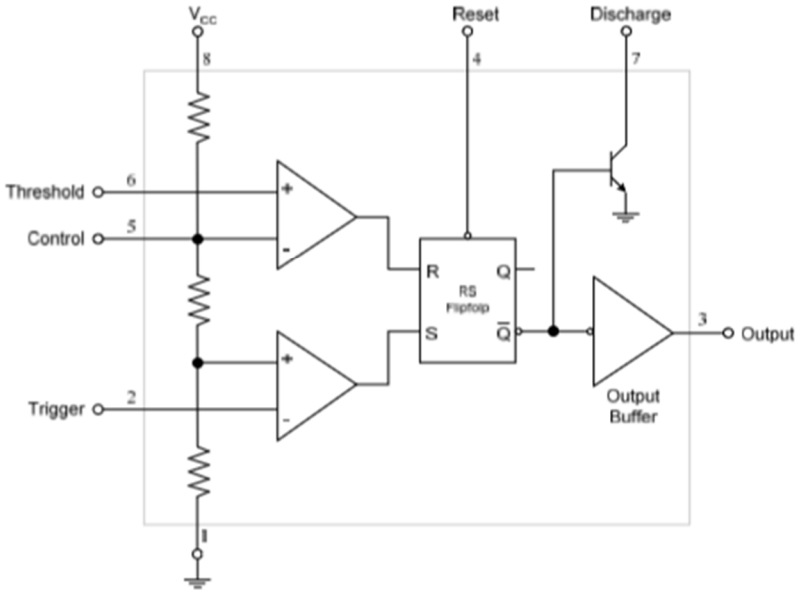


Fig2:IC 555 Functional block diagram

Astablemultivibrator using IC 555

One popular application of the 555 timer IC is as an astablemultivibrator or clock Circuit. Figure 3 shows an astable circuit built using 2 external resistors and a capacitor to set the timing interval of the output signal. Capacitor C charges toward VCC through external resistors RA and RB. Referring to figure, the capacitor voltage rises until it goes above 2/3 VCC . This voltage is the threshold voltage at pin 6, which drives comparator 1 to trigger the flipflop(Q low Q'high) so that the output at pin 3 goes low. In addition, the discharge transistor is driven on, causing the output at pin 7 to discharge the capacitor through resistor RB. The capacitor voltage then decreases until it drops below the trigger level 1/3 VCC . The flipflop is triggered so that the output goes back high and the discharge transistor is turned off, so that the capacitor can again charge through resistors RA and RB towards VCC.

CIRCUIT DIAGRAM & DESIGN

Take $V = 10V$ and f = 1000 Hz and duty cycle = 60 % Then t = 1 ms, t_H = 0.6 ms, t_L = 0.4 ms

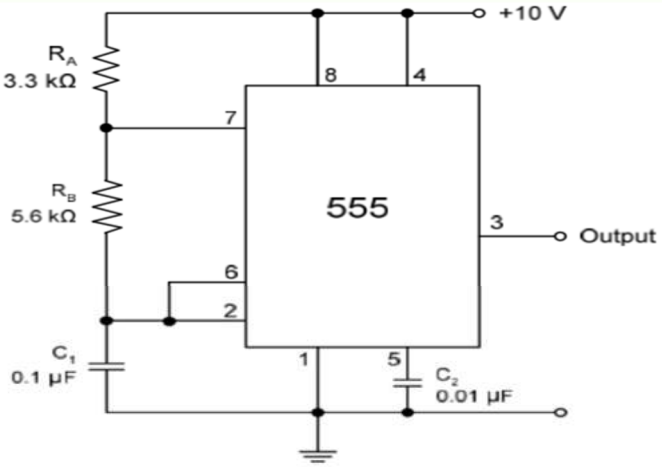


Figure 3 Astable multivibrator circuit using IC 555

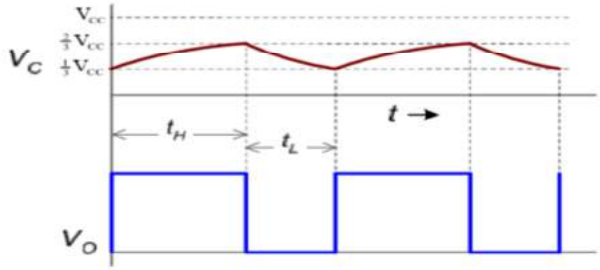


Figure 4 Waveforms of voltage across the capacitor and output voltage

Assume C = 0.1 μF

t_l=0.693.*R*Cthen R_B = 5.77 kΩtake R_B = 5.6 kΩ

t_r=0.6393*(R_A+R_B)*Cthen R_A = 3.06kΩtake R_B = 3.3kΩ

The resistance R_A and R_B should be in the range of 1k to 10k to limit the collector current of the internal transistor.

Procedure:

1. Set up the circuit after verifying the condition of IC

2. Observe the waveforms at pin number 3 and 6 of the IC

Result:

Astablemultivibrator using timer IC 555 is designed and setup, and the waveforms are obtained.

Table 1: Observation of AstableMultivibrator.

S No	R_2	Theoretical Calculated frequency	Pulse T_{ON}	Pulse T_{OFF}	Period, T $T_{ON} + T_{OFF}$	Frequency, f (1/T)	Duty cycle T_{ON} / T
1	1kΩ						
2	100 kΩ						
3	1 MΩ						

Conclusion:

Experiment 6

AIM: To design anmonostablemultivibrator of given specifications using 555 Timer.

Apparatus:

1. 555 IC Timer
2. Resistor - 10 KΩ
3. Capacitors- 10nF, 0.1µF, 0.01µF
4. Function Generator-1MHz
5. CRO-20 MHz
6. Bread Board
7. Connecting Wires and Probes

Theory:

It has one stable and one quasi stable state. The circuit is useful for generating single output pulse of time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. The diode gives a negative triggering pulse. When the output is +Vsat, a diode clamps the capacitor voltage to 0.7V then, a negative going triggering impulse magnitude Vi passing through RC and the negative triggering pulse is applied to the positive terminal. Let us assume that the circuit is instable state. The output V0i is at +Vsat. The diode D1 conducts and Vc the voltage across the capacitor 'C' gets clamped to 0.7V,the voltage at the positive input terminal through R1R2 potentiometer divider is +ßVsat. Now, if a negative trigger of magnitude Vi is applied to the positive terminal so that the effective signal is less than 0.7V.the output of the Op-Amp will switch from +Vsat to –Vsat. The diode will now get reverse biased and the capacitor starts charging exponentially to –Vsat. When the capacitor charge Vc becomes slightly more negative than –ßVsat, the output of the op-amp switches back to +Vsat. The capacitor 'C' now starts charging to +Vsat through R until Vc is 0.7V.

V0 = Vf + (Vi-Vf) $e^{t/R}$, ß = R2/(R1+R2)

If Vsat>>Vp and R1=R2 and ß = 0.5,

Then, T = 0.69RC

Circuit Diagram:

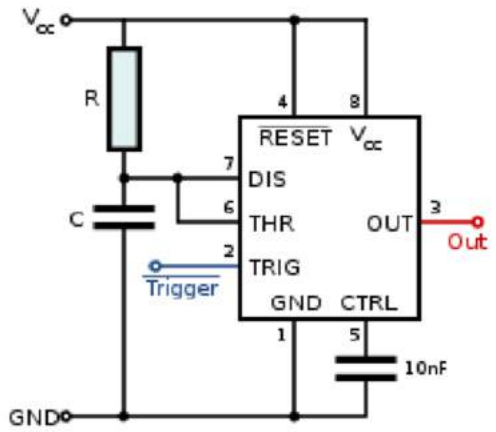


Figure 1: MonostableMultivibrator

Procedure:

1. Connect the circuit as shown in the circuit diagram.

2. Apply Negative triggering pulses at pin 2 of frequency 1 KHz as shown in Fig.

3. Observe the output waveform and capacitor voltage as shown in Figure and measure the pulse duration.

4. Theoretically calculate the pulse duration as T_{high} =1.1 RC

5. Compare it with experimental values.

Observation: Trace the time period of the output wave form and compare it with the given one.

Result & Discussion: The waveform is observed and verified with stated condition.